

Dhruv Patel

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Profile

Computer Engineering student at Iowa State University with 3+ years of experience in analog and digital circuit design, embedded systems, and computer architecture. Skilled in circuit simulation, hardware testing, and tools such as VHDL/Verilog, CAD tools, and MATLAB.

Education

Iowa State University

Bachelor of Science in Computer Engineering (GPA: 3.73/4)

Bachelor of Science in Cyber Security (Minor)

Ames, IA, United States

Aug. 2025 – Present

Nirma University

Bachelor of Science in Computer Science (GPA: 8.5/10)

Ahmedabad, GJ, India

Jul. 2023 – Jun. 2025

Relevant Coursework: Integrated Circuits, Embedded Systems, Computer Organization and Architecture, Data Structures, Operating Systems, Cyber Security Fundamentals and Tools, Software Development Practices, Algorithms, Electric Circuits and Systems.

Technical Skills

Programming Languages: Bash, Java, HTML, JavaScript, C, C++, SQL, Assembly, Verilog, VHDL.

Hardware and Platforms: ESP32, Arduino, MSP430, ARM-based microcontroller, FPGA development, Sensor and Actuator Interfacing, Digital Logic Implementation.

Design and Simulation Tools: Cadence Virtuoso, QuestaSim/ModelSim, Quartus Prime, VS Code, TensorFlow, NumPy, Pandas, OpenCV, Code Composer Studio, MATLAB, LTspice, Git.

Circuits and Knowledge: Analog and Digital Circuit Design, Op-Amp Circuits, RISC-V, Basic CMOS/VLSI, Hardware Testing and Debugging.

Security Tools and Standards: Nmap, Wireshark.

Operating Systems: Windows 10/11, MacOS, Kali Linux, Ubuntu, Red Hat Linux.

Other Skills & Tools: Datasheet Analysis, Schematic Interpretation, Technical Documentation, Hardware–Software Integration, System Testing, Deep Learning, Machine Learning, Neural Networks, Image Processing, Data Analysis.

Honors

Tau Sigma National Honor Society, Iowa State University (2026)

Dean's List, Iowa State University (Fall 2025, Spring 2026)

Experience

Undergrad Teaching Assistant

Iowa State University

Jan. 2026 – Present

Ames, IA, United States

- Guide students in designing, implementing, and debugging digital logic circuits using Verilog and FPGA-based development tools.
- Provide technical support during lab sessions by explaining combinational and sequential logic concepts and troubleshooting hardware and simulation issues.

UnderGrad Research Assistant

Iowa State University

May 2026 – Present

Ames, IA, United States

- Assist in developing robust electronic circuits for detecting and assessing lameness in cows, supporting improved animal health and welfare.
- Design impedance-measurement circuits to estimate body mass, muscle composition, and fat ratios in pigs.

Projects and Research

AI-Based Parkinson's Disease Classification from MRI | Machine Learning, Deep Learning

May. 2024 – Dec. 2025

- Developed and trained deep learning models to classify Parkinson's disease using 2D and 3D MRI data from the PPMI dataset.
- Applied generative techniques (GANs, VAEs, Diffusion) to create synthetic MRI images, improving dataset size and enhancing model performance and generalization.

Remote-Operated Robotic Tank Simulation | Tiva-C (ARM), Embedded C

Nov. 2025 – Dec. 2025

- Developed a remote-controlled robotic system integrating ultrasonic, IR, IMU sensors, and servo control for navigation and target detection.
- Implemented UART and I²C communication for real-time user control and multi-microcontroller coordination, along with a GUI for system monitoring and status visualization.